wherein the step of forming the element isolation groove includes another step of forming an other element isolation groove adjacent to the element isolation groove in a region other than an element formation region of the semiconductor layer,

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wherein in the step of forming the third insulating film, the third insulating film is formed such that the element isolation groove and the other element isolation groove are continuously covered, and

wherein the second insulating film and the third insulating film are composed of SiO_2.

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application..

Claims 1, 4, and 5 are pending in the instant application, of which claims 1 is independent.

Turning now to the Office Action, claim 1, and 4-5 are rejected under 35 U.S.C. §102(b) as anticipated by Razouk (U.S. Patent No. 5,581,110). In view of the amendments above and the remarks provided below, reconsideration and withdrawal of the rejection is respectfully requested.

As amended, claim 1 further recites the second insulating film and the third insulating film are composed of SiO_2. The amended claim 1 of the present invention and the disclosed invention of Razouk are different as follows:

1) the third insulating film (i.e., the cap 109 of the embedded polysilicon, PS, 108) in the present invention is composed of SiO_2, while in Razouk the nitride layer 1302, shown in Fig. 13, is composed of SiN; and

2) the film composition from the embedded polysilicon 108 to sidewalls of the trench in the present invention, as shown in, e.g., Fig. 11, is PS/SiO_2 (second insulating film)/SiO_2/Si (device region), while that in Razouk is PS/SiN/SiO_2/Si (device region).

The above differences are due to the reason that the SiN film (702, 1302) that covers the polysilicon 802 of Razouk also functions as an oxygen barrier and does not merely function as an insulating film such as the second or the third insulating film of the present invention.

Due to the above structure/composition differences, the effects of the present invention and that of Razouk are different as follows:

(A) with respect to 1), since the dielectric constant of SiN is larger than that of SiO_2, the parasitic capacitance of the (metal) wire formed on the trench tends to be larger, and the operation speed of the device decreases. In other words, in the case of Razouk, a parasitic capacitance element having a composition of PS/SiN/LTO (low temperature silicon dioxide layer)/(metal) wire is possible; and

(B) with respect to 2), since the film composition of Razouk is PS/SiN/SiO_2/Si (device region), Razouk discloses a MNOS (Metal Nitride Oxide Semiconductor) structure. Attached herewith is a reference to Kamigaki ("MNOS Nonvolatile Semiconductor Memory Technology: Present and Future", *IEICE Trans. Electron*, Vol. E84-C, No. 6, June 2001) relating to the MNOS technology. As can be seen, the MNOS structure is well known for having numerous levels that trap charges in the interfaces of SiN/SiO_2 (and SiN). Since charges are trapped during operation, there is a possibility that the characteristic of the device becomes unstable.

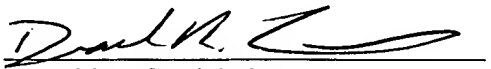
Specifically, it is uncertain what the electric potential of the PS would become under the influence of the above parasitic MNOS including trapped charges. As a result, what the parasitic capacitance element of (A) becomes would also be uncertain, and the influence on the (metal) wiring would also be uncertain. Hence, Applicants respectfully assert that, in Razouk, the problem of malfunction of device would occur due to the conditional charging and discharging of charges.

On the other hand, since the presently claimed invention is not influenced by the parasitic capacitance and parasitic MNOS of Razouk, an excellent device operation can be achieved.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Razouk, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1, and 4-5, under 35 U.S.C. § 102(b), as anticipated by Razouk would be improper.

Having responded to the rejection set forth in the outstanding Final Office Action, it is submitted that independent claim 1, and dependent claims 4-5 are in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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MARKED-UP COPY OF AMENDED CLAIM:

1. (Twice Amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming, in a semiconductor layer formed on a first insulating film, an element isolation groove extending to the first insulating film;

depositing a second insulating film so as to partially fill the element isolation groove by using a vapor deposition method;

forming an embedded layer on the second insulating film so as to completely fill the element isolation groove; and

forming a third insulating film on the embedded layer [using the vapor deposition method],

wherein the step of forming the element isolation groove includes another step of forming an other element isolation groove adjacent to the element isolation groove in a region other than an element formation region of the semiconductor layer, [and]

wherein in the step of forming the third insulating film, the third insulating film is formed such that the element isolation groove and the other element isolation groove are continuously covered, and

wherein the second insulating film and the third insulating film are composed of SiO_2.